REMARKS

The Office Action dated April 25, 2005 has been carefully considered. Claims 1-9 are pending. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 1-2 and 4-9 have been amended in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and the following remarks.

An interview was held with the Examiner, Mr. David C. Mis, on June 9, 2005, to discuss the rejections under 35 U.S.C. § 102(b) and the proposed amendments thereto. Applicants wish to thank the Examiner for his time and the courtesies extended.

Claims 5, 8 and 9 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Insofar as these rejections may be applied against the amended claims, they are deemed overcome.

Amended Claim 5 describes "a variable impedance damping resistor *which is* part of said LPF." Accordingly, the LPF (low pass filter) of amended Claim 5 contains the variable impedance damping resistor. Amended Claim 8 describes "a feedback clock signal *having a corresponding W1 frequency component signal*" and an "LPF including a switched capacitor circuit with a control signal input." Accordingly, the feedback clock signal with a W1 component is used to provide the control signal input of the switched capacitor circuit. Amended Claim 9 describes an LPF that receives "*an* output of *a* mixer" and "a variable impedance damping resistor *which is* part of said LPF." Accordingly, the LPF of amended Claim 9 contains the variable impedance damping resistor. Applicants respectfully request that the rejections of Claims 5, 8 and 9 under 35 U.S.C. § 112, second paragraph be withdrawn and that amended Claims 5, 8 and 9 be allowed.

Claims 1, 4 and 8 stand rejected under 35 U.S.C. § 102(b) in view of U.S. Patent 4,007,429 to Cadalora et al. ("Cadalora"). Insofar as these rejections may be applied against the amended claims, they should be deemed overcome.

Claim 1 has been amended to clarify a feature of the present invention. The method of amended Claim 1 describes "switching the switched capacitance, as a function of a reference frequency and *a divided* PLL (phase lock loop) output frequency *wherein said function is a substantially continuous difference between the reference frequency and the divided PLL output frequency.*" Support for this amendment can be found, among other places, page 6, lines 3-24 of the original Application.

The Cadalora reference does not teach, suggest, or disclose this feature of the present invention. Specifically, Cadalora discloses a method of varying the loop bandwidth of a PLL by using a switched lowpass filter having a first bandwidth with a wide frequency response for rapid acquisition of a frequency and a second bandwidth with a narrow frequency response for tight control of a frequency. Cadalora does not disclose switching the switched capacitance as a function of a difference between a reference frequency and the divided PLL output frequency. This feature enables the present invention to acquire a desired frequency much quicker. Accordingly, when the reference frequency and the output frequency are substantially different, the switched capacitance creates a large resistance and the voltage to the VCO (voltage controlled oscillator) is affected dramatically, which affects the output frequency dramatically. As the PLL output frequency evens out with the reference frequency, the divided PLL output frequency creates a small resistance for the switched capacitance and the voltage to the VCO remains substantially the same and the desired frequency is acquired. It is clear that this feature of the present invention is not disclosed by the Cadalora reference.

In view of the foregoing, it is apparent that the cited reference does not disclose, teach or suggest the unique combination now recited in amended Claim 1. Applicants therefore submit that amended Claim 1 is both clearly and precisely distinguishable over the cited reference in a patentable sense. Accordingly, Applicants respectfully request that the rejection of Claim 1 under 35 U.S.C. § 102(b) in view of Cadalora be withdrawn and that amended Claim 1 be allowed.

Claim 4 has been amended to clarify a feature of the present invention. The method of amended Claim 4 describes "generating a switching signal that is a function of a reference frequency and *a divided* PLL output frequency *wherein said function is a substantially continuous difference between the reference frequency and the divided PLL output frequency.*" Support for this amendment can be found, among other places, page 6, lines 3-24 of the original Application.

The Cadalora reference does not teach, suggest, or disclose this feature of the present invention. Specifically, Cadalora discloses a method of varying the loop bandwidth of a PLL by using a switched lowpass filter having a first bandwidth with a wide frequency response for rapid acquisition of a frequency and a second bandwidth with a narrow frequency response for tight control of a frequency. Cadalora does not disclose switching the connections of a switched capacitor as a function of the switching signal that is a function of a difference between the reference frequency and the divided PLL output frequency. This feature enables the present invention to acquire a desired frequency much quicker. Accordingly, when the reference frequency and the output frequency are substantially different, the switched capacitor creates a large resistance and the voltage to the VCO (voltage controlled oscillator) is affected dramatically, which affects the output frequency dramatically. As the PLL output frequency evens out with the reference frequency, the divided PLL output frequency creates a small resistance for the switched capacitance

and the voltage to the VCO remains substantially the same and the desired frequency is acquired. It is clear that this feature of the present invention is not disclosed by the Cadalora reference.

In view of the foregoing, it is apparent that the cited reference does not disclose, teach or suggest the unique combination now recited in amended Claim 4. Applicants therefore submit that amended Claim 4 is both clearly and precisely distinguishable over the cited reference in a patentable sense. Accordingly, Applicants respectfully request that the rejection of Claim 4 under 35 U.S.C. § 102(b) in view of Cadalora be withdrawn and that amended Claim 4 be allowed.

Claim 8 has been amended to clarify a feature of the present invention. The method of amended Claim 8 describes "a difference means for developing a control signal corresponding to *a substantially continuous* difference between W2 and W1 frequency component signals, said control signal being delivered to said control input of said switched capacitor circuit." Support for this amendment can be found, among other places, page 6, lines 3-24 of the original Application.

The Cadalora reference does not teach, suggest, or disclose this feature of the present invention. Specifically, Cadalora discloses a method of varying the loop bandwidth of a PLL by using a switched lowpass filter having a first bandwidth with a wide frequency response for rapid acquisition of a frequency and a second bandwidth with a narrow frequency response for tight control of a frequency. Cadalora does not disclose switching the switched capacitance as a function of a substantially continuous difference between a reference clock input and the feedback clock signal. This feature enables the present invention to acquire a desired frequency more rapidly. It is clear that this feature of the present invention is not disclosed by the Cadalora reference.

In view of the foregoing, it is apparent that the cited reference does not disclose, teach or suggest the unique combination now recited in amended Claim 8. Applicants therefore submit that amended Claim 8 is both clearly and precisely distinguishable over the cited reference in a

patentable sense. Accordingly, Applicants respectfully request that the rejection of Claim 8 under 35 U.S.C. § 102(b) in view of Cadalora be withdrawn and that amended Claim 8 be allowed.

Claims 7 and 9 stand rejected under 35 U.S.C. § 102(b) in view of U.S. Patent 5,202,924 to Richards et al. ("Richards"). Insofar as these rejections may be applied against the amended claims, they should be deemed overcome.

Claim 7 has been amended to clarify a feature of the present invention. The LPF of Claim 7 contains "a variable impedance damping resistor, the impedance of said variable impedance damping resistor varying as a function of *a difference between* F1 *and the signal frequency divider output*." Support for this amendment can be found, among other places, page 6, lines 3-24 of the original Application.

The Richards reference does not teach, suggest or disclose this feature of the present invention. Specifically, Richards discloses a stereo decoder wherein a phase comparator receives a reference signal and an output signal of the VCO where its frequency is divided by two. In contrast with Richards, the present invention employs a signal frequency divider that alters the frequency of the VCO output signal by a ratio of F1 and F2, wherein F1 is the frequency of a reference signal and F2 is the desired output frequency of the PLL. Then, an impedance of a variable impedance damping resistor varies as a function of the difference between F1 and the output of a signal frequency divider output. Accordingly, the reference signal is operable on the frequency of the VCO output signal and is used again to vary the impedance of the variable impedance damping resistor. This feature of the present invention enables the present invention to acquire a desired frequency much quicker than Richards.

In view of the foregoing, it is apparent that the cited reference does not disclose, teach or suggest the unique combination now recited in amended Claim 7. Applicants therefore submit that

amended Claim 7 is both clearly and precisely distinguishable over the cited reference in a patentable sense. Accordingly, Applicants respectfully request that the rejection of Claim 7 under 35 U.S.C. § 102(b) in view of Richards be withdrawn and that amended Claim 7 be allowed.

Claim 9 has been amended to clarify a feature of the present invention. The control signal applying means of Claim 9 provides "a control signal F1 indicative of *a* difference *between the reference clock input and the feedback clock input.*" Support for this amendment can be found, among other places, page 6, lines 3-24 of the original Application.

The Richards reference does not teach, suggest or disclose this feature of the present invention. Specifically, Richards discloses a stereo decoder wherein a phase comparator receives a reference signal and an output signal of the VCO. In contrast with Richards, the present invention employs an independent control signal supplying means that produces a control signal indicative of a difference between the reference clock input and the feedback clock input. Then, an impedance of a variable impedance damping resistor varies as a function of this difference. Therefore, the PFD (phase frequency detector) applies a comparison between the reference clock input and the feedback clock input while the control signal adjusts the impedance of the variable impedance damping resistor. This feature of the present invention enables the present invention to acquire a desired frequency much quicker than Richards.

In view of the foregoing, it is apparent that the cited reference does not disclose, teach or suggest the unique combination now recited in amended Claim 9. Applicants therefore submit that amended Claim 9 is both clearly and precisely distinguishable over the cited reference in a patentable sense. Accordingly, Applicants respectfully request that the rejection of Claim 9 under 35 U.S.C. § 102(b) in view of Richards be withdrawn and that amended Claim 9 be allowed.

Claims 2, 3 and 6 are objected to as being dependent upon a rejected claim. Claims 2 and 3 depend upon and further limit amended Claim 1 and Claim 6 depends upon and further limits amended Claim 5. Hence, for at least the aforementioned reasons, these Claims should be deemed to be in condition for allowance. Accordingly, Applicants respectfully request that the objections to dependent Claims 2, 3 and 6 also be withdrawn.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-9.

Applicants do not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

Dated: 7/25/05

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